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IMPLEMENTATION OF LOW-COMPLEXITY TURBO DECODER FOR WIRELESS SENSOR NETWORKS

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ABSTRACT

Energy consumption wireless networks the Turbo codes are mostly used, It has very low transmission energy consumption. To decrease transmission energy consumption, lookup table-log-BCJR (LUT-Log-BCJR) architectures produce small dispensation energy utilization is required. In this paper, we molder the LUT-Log-BCJR structural design change most of essential add compare select (ACS) operations and execute using a novel low-complexity ACS unit. We show the structural design of extent fewer gates, current LUT-Log-BCJR architectures, assisting 71% energy utilization decrease. Evaluate the modern maximum logarithmic Bahl-Cocke-Jelinek-Raviv method; our advanced design smooths the progress of a 10% reduction in the overall energy utilization when the range above 60 m.

KEY WORDS
BCJR, ACS, Wireless Sensor Network and ACS.
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INTRODUCTION[1]

The Wireless Sensor Networks (WSNs)[1-3] can be considered to be energy constrained wireless scenarios since the sensors are operated for extended periods of time, while relying on batteries that are small, lightweight and inexpensive. The Max-Log-BCJR algorithm appears to lend itself to both high-throughput scenarios, as well as to the above-mentioned energy-constrained scenarios. This is because low turbo decoder energy consumption is implied by Max-Log-BCJR algorithm's low

complexity. However, this is achieved at the cost of degrading the coding gain by 0.5 dB compared to the optimal Log-BCJR algorithm increasing the required transmission energy by 10%. As we shall demonstrate in Section IV, this disadvantage of the Max-Log-BCJR outweighs its attractively low complexity, when optimizing the overall energy consumption of sensor nodes that are separated by dozens of meters.

PROBLEM ANALYSIS

1. The energy-constrained scenarios, since it approximates the optimal Log-BCJR more closely than the Max-Log-BCJR and therefore does not suffer from the associated coding gain degradation.
2. This motivates our novel architecture of which is specifically designed to have a minimal hardware complexity and hence a low energy consumption.
3. Each of these windows is generated separately, using a forward, a pre-backward and a backward recursion.

IMPLIMENTATION METHOD

The propose a novel LUT-Log-BCJR architecture for energy-constrained scenarios, which avoids the wastage of energy that is inherent in the conventional architecture. Our philosophy is to redesign the timing of the conventional architecture in a manner that allows its components to be efficiently merged. This produces an architecture comprising only a low number of inherently low-complexity functional units, which are collectively capable of performing the entire LUT-Log-BCJR algorithm. Further wastage is avoided, since the critical paths of our functional units are naturally short and equally-lengthened, eliminating the requirement for additional hardware to manage them. Furthermore, our approach naturally results in a low area and a high clock frequency, which implies low static energy consumption. As we will show in the LUT-Log-BCJR algorithm is naturally suited to this philosophy, since it can be decomposed into classic ACS operations. In we tackle the challenge of devising an architecture that is sufficiently flexible for performing the entire LUT-Log-BCJR algorithm, using only a small number of functional units.

Advantages

1. The proposes a functional unit that is capable of performing ACS operations, while maintaining a short critical path and a low complexity. Finally, we will design a controller for our architecture, using the LUT-Log-BCJR decoder of the 3GPP LTE turbo decoder as an application.
2. These alternative algorithms reduce the hardware complexity and increase the throughput, therefore reducing the energy consumption.

METHOD VALIDATION[4-8]

Energy-Efficient LUT-Log-BCJR

The proposed energy- efficient LUT-Log-BCJR architecture is unlike conventional architectures, it does not use separate dedicated hardware for the three recursions. Instead, our architecture implements the entire algorithm using ACS units in parallel, each of which performs one ACS operation per clock cycle. Furthermore, the proposed architecture employs a twin-level register structure to minimize the highly energy-consuming main-memory access operations (Figure No.1).

Controller Design

The proposed architecture can be readily applied to any LUT-Log-BCJR decoder, regardless of the corresponding convolution encoder parameters employed. This is achieved by specifically designing a controller for the LUT-Log-BCJR decoder. To exemplify this, we designed a controller for a sliding-window implementation of the LTE turbo code's LUT-Log-BCJR decoder, which corresponds to an encoder having memory elements. Since the proposed architecture employs parallel ACS units, it facilitates the parallel processing of or state metrics at a time.

Dynamic energy consumption

The dynamic energy consumption, the reduced throughput implies increased static energy consumption, particularly in the case of high-density technologies. Furthermore, the lengthening of the critical path implies a greater variety of path lengths,

particularly since the backward recursion path is significantly longer than those of the other recursions. This in turn implies that a greater fraction of the static energy consumption can be considered to be wasted, by giving short data paths more time to settle than necessary. In summary, efforts to slow down the conventional LUT-Log-BCJR architecture result in energy wastage, which cannot be avoided without completely redesigning the architecture.

LUT-Log-BCJR Architecture[9]

A number of variants of the LUT-Log-BCJR architecture of have been proposed for further increasing the decoding throughput. For example, employs parallel repetitions of the blocks to "parallel-process" the schedule. Alternatively, employs a radix-4 variant, which processes two sets of or state metrics at a time. In summary, conventional LUT-Log-BCJR architectures achieve high throughputs by employing substantial hardware, which imposes a high chip area and consequently high energy consumption, as quantified later.

Low Energy Consumption

This motivates our novel architecture of which is specifically designed to have a minimal hardware complexity and hence a low energy consumption. We validate our architecture in the context of an LTE turbo decoder and demonstrate that it has an order of magnitude lower chip area, hence reducing the energy consumption of the state-of-the-art LUT-Log-BCJR implementation by 71%. Compared to state-of-the-art Max-Log-BCJR implementations, our approach facilitates a 10% reduction[10].

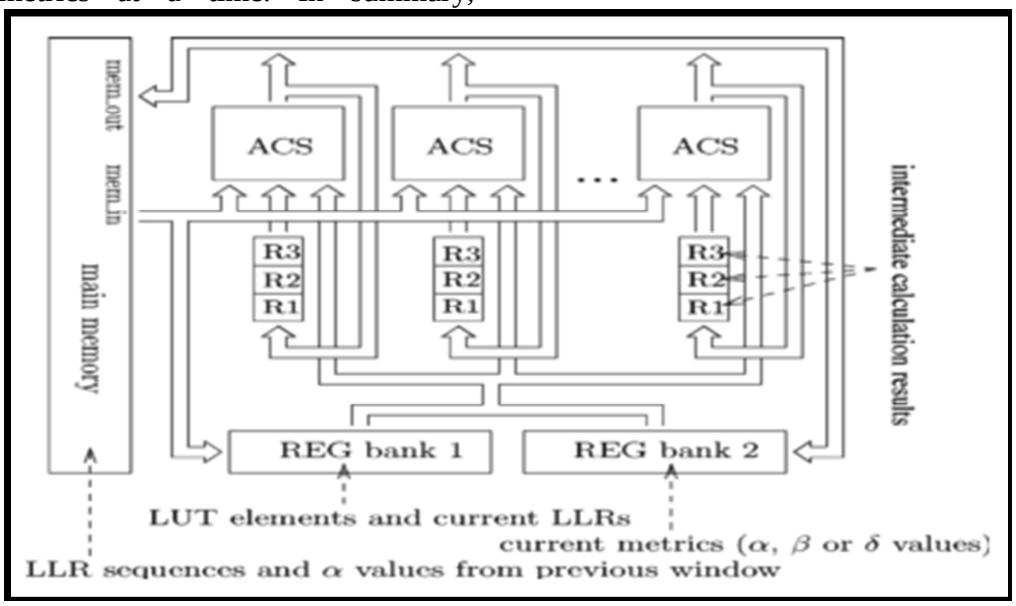

Figure No.1: Flow Diagram: Energy-Efficient LUT-Log- BCJR Architecture

CONCLUSION

In this paper, we demonstrated that upon aiming for a high throughput, conventional LUT-Log-BCJR architectures may have wasteful designs requiring high chip areas and hence high energy consumptions. However, in energy-constrained applications, achieving low energy consumption has a higher priority than having a high throughput. This motivated our low-complexity energy-efficient architecture, which achieves a low area and hence a low energy consumption by decomposing the LUT-Log-BCJR algorithm into its most fundamental ACS operations. In addition, the proposed architecture may be readily reconfigured for different turbo codes or decoding algorithms. We validated the architecture by implementing an LTE turbo decoder, which was found, in Table III, to have an order-of-magnitude lower area than conventional LUT-Log-BCJR decoder implementations and an approximately 71% lower energy consumption of 0.4 nJ/bit/iteration. Compared to state of the art Max-Log-BCJR implementations, our approach facilitates

a 10% reduction in the overall energy consumption at transmission ranges above 58 m. Furthermore, we demonstrated that our implementation has a throughput of 1.03 Mb/s, which is appropriate for energy-constrained applications, such as in environmental monitoring WSNs.

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CONFLICT OF INTEREST

We declare that we have no conflict of interest.

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